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Additional information on the models, ports, and options can be obtained from UG196, Virtex-5 FPGA RocketIO GTP Transceiver User Guide. Additional information regarding the Quantum Channel Designer

can be obtained from the SiSoft Quantum Channel Designer User Guide (provided with the SIS Kit installation). Page 8: Installation And Requirements

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(This parameter is basically the hysteresis for logic ‘0’.) VIH(max) must not exceed 1.9V for all Micron Parts. www.xilinx.com Virtex-5 FPGA ML561 User Guide UG199 (v1.2.1) June 15, 2009...

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For 3.3V I/O operation, refer to UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines. 5. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond

the normal specification for no mor e than 20% of a data period .

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The LUTs in Virtex-5 FPGAs can be configured as either 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Four such

LUTs and four flip flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a Configurable Logic Block (CLB).

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This book describes the optimized implementations of several arithmetic datapath, controlpath and pseudorandom sequence generator circuits for realization of high performance arithmetic circuits targeted towards a specific family of the high-end Field Programmable Gate Arrays (FPGAs). It explores regular, modular, cascadable and bit-sliced architectures of these circuits, by directly instantiating the target FPGA-specific primitives in the HDL. Every proposed architecture is justified with detailed mathematical analyses. Simultaneously, constrained placement of the circuit building blocks is performed, by placing the logically related hardware primitives in

close proximity to one another by supplying relevant placement constraints in the Xilinx proprietary “User Constraints File”. The book covers the implementation of a GUI-based CAD tool named FlexiCore integrated with the Xilinx Integrated Software Environment (ISE) for design automation of platform-specific high-performance arithmetic circuits from user-level specifications. This tool has been used to implement the proposed circuits, as well as hardware implementations of integer arithmetic algorithms where several of the proposed circuits are used as building blocks. Implementation results demonstrate higher performance and superior operand-width scalability for the proposed circuits, with respect to implementations derived through other existing approaches. This book will prove useful to researchers, students and professionals engaged in the domain of FPGA circuit optimization and implementation.

This book is designed both for FPGA users interested in developing new, specific components - generally for reducing execution times -and IP core designers interested in extending their catalog of specific components. The main focus is circuit synthesis and the discussion shows, for example, how a given algorithm executing some complex function can be translated to a synthesizable circuit description, as well as which are the best choices the designer can make to reduce the

circuit cost, latency, or power consumption. This is not a book on algorithms. It is a book that shows how to translate efficiently an algorithm to a circuit, using techniques such as parallelism, pipeline, loop unrolling, and others. Numerous examples of FPGA implementation are described throughout this book and the circuits are modeled in VHDL. Complete and synthesizable source files are available for download.

It gives me immense pleasure to introduce this timely handbook to the research/- velopment communities in the ?eld of signal processing systems (SPS). This is the ?rst of its kind and represents state-of-the-arts coverage of research in this ?eld. The driving force behind information technologies (IT) hinges critically upon the major advances in both component integration and system integration. The major breakthrough for the former is undoubtedly the invention of IC in the 50's by Jack S. Kilby, the Nobel Prize Laureate in Physics 2000. In an integrated circuit, all components were made of the same semiconductor material. Beginning with the pocket calculator in 1964, there have been many increasingly complex applications followed. In fact, processing gates and memory storage on a chip have since then grown at an exponential rate, following Moore's Law. (Moore himself admitted that Moore's Law had turned out to be more accurate, longer

lasting and deeper in impact than he ever imagined.) With greater device integration, various signal processing systems have been realized for many killer IT applications. Further breakthroughs in computer sciences and Internet technologies have also catalyzed large-scale system integration. All these have led to today's IT revolution which has profound impacts on our lifestyle and overall prospect of humanity. (It is hard to imagine life today without mobiles or Internets!) The success of SPS requires a well-concerted integrated approach from mul- ple disciplines, such as device, design, and application.

A series of cogently written articles by 49 industry experts, this collection fills the void on Power Distribution Network (PDN) design procedures, and addresses such related topics as DC-DC converters, selection of bypass capacitors, DDR2 memory systems, powering of FPGAs, and synthesis of impedance profiles. Through these contributions from such leading companies as Sun Microsystems, Sanyo, IBM, Hewlett-Packard, Intel, and Rambus, readers will come to understand why books on power integrity are only now becoming available to the public and can relate these topics to current industry trends.

Reconfigurable computing brings immense flexibility to on-chip processing while network-on-chip has improved flexibility in on-chip communication. Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems-on-chip. This book is the one of the first compilations written to demonstrate this future for network-on-chip design. Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques, to task assigning, scheduling and arrival, to designing an operating system to take advantage of the computing and communication flexibilities brought about by run-time reconfiguration and network-on-chip, it represents a complete source of the techniques and applications for reconfigurable network-on-chip necessary for understanding of future of this field.

Rapid energy estimation for energy efficient applications using field-programmable gate arrays (FPGAs) remains a challenging research topic. Energy dissipation and efficiency have prevented the widespread use of FPGA devices in embedded systems, where energy efficiency is a key performance metric. Helping overcome these challenges, Energy Efficient Hardware-Software Co-Synthesis Using Reconfigurable Hardware offers solutions for the development of energy efficient applications using FPGAs. The book integrates various high-level abstractions for

describing hardware and software platforms into a single, consistent application development framework, enabling users to construct, simulate, and debug systems. Based on these high-level concepts, it proposes an energy performance modeling technique to capture the energy dissipation behavior of both the reconfigurable hardware platform and the target applications running on it. The authors also present a dynamic programming-based algorithm to optimize the energy performance of an application running on a reconfigurable hardware platform. They then discuss an instruction-level energy estimation technique and a domain-specific modeling technique to provide rapid and fairly accurate energy estimation for hardware-software co-designs using reconfigurable hardware. The text concludes with example designs and illustrative examples that show how the proposed co-synthesis techniques lead to a significant amount of energy reduction. This book explores the advantages of using reconfigurable hardware for application development and looks ahead to future research directions in the field. It outlines the range of aspects and steps that lead to an energy efficient hardware-software application synthesis using FPGAs.

Reconfigurable Computing Systems Engineering: Virtualization of Computing Architecture describes the organization of reconfigurable

computing system (RCS) architecture and discusses the pros and cons of different RCS architecture implementations. Providing a solid understanding of RCS technology and where it's most effective, this book: Details the architecture organization of RCS platforms for application-specific workloads Covers the process of the architectural synthesis of hardware components for system-on-chip (SoC) for the RCS Explores the virtualization of RCS architecture from the system and on-chip levels Presents methodologies for RCS architecture run-time integration according to mode of operation and rapid adaptation to changes of multi-parametric constraints Includes illustrative examples, case studies, homework problems, and references to important literature A solutions manual is available with qualifying course adoption. Reconfigurable Computing Systems Engineering: Virtualization of Computing Architecture offers a complete road map to the synthesis of RCS architecture, exposing hardware design engineers, system architects, and students specializing in designing FPGA-based embedded systems to novel concepts in RCS architecture organization and virtualization.

This book constitutes the thoroughly refereed post-proceedings of the 17th Annual International Workshop on Selected Areas in Cryptography, SAC 2010, held in Waterloo, Ontario, Canada in August 2010. The 24

revised full papers presented together with 2 invited papers were carefully reviewed and selected from 90 submissions. The papers are organized in topical sections on hash functions, stream ciphers, efficient implementations, coding and combinatorics, block ciphers, side channel attacks, and mathematical aspects.

This book explains the application of recent advances in computational intelligence - algorithms, design methodologies, and synthesis techniques - to the design of integrated circuits and systems. It highlights new biasing and sizing approaches and optimization techniques and their application to the design of high-performance digital, VLSI, radio-frequency, and mixed-signal circuits and systems. This second of two related volumes addresses digital and network designs and applications, with 12 chapters grouped into parts on digital circuit design, network optimization, and applications. It will be of interest to practitioners and researchers in computer science and electronics engineering engaged with the design of electronic circuits.

This book constitutes the refereed proceedings of the Cryptographers' Track at the RSA Conference 2012, CT-RSA 2012, held in San Francisco, CA, USA, in February/March 2012. The 26 revised full papers presented

were carefully reviewed and selected from 113 submissions. The papers are organized in topical sections on side channel attacks, digital signatures, public-key encryption, cryptographic protocols, secure implementation methods, symmetric key primitives, and secure multiparty computation.

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